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MICRON TECHNOLOGY, INC.

**UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA**

MICRON TECHNOLOGY, INC.,

Plaintiff,

v.

UNITED MICROELECTRONICS
CORPORATION, FUJIAN JINHUA
INTEGRATED CIRCUIT CO., LTD.,
and DOES 1-10,

Defendants.

Case No. 4:17-CV-06932-MMC

**DECLARATION OF DAVID LIU, PH.D. IN
SUPPORT OF MICRON TECHNOLOGY,
INC.'S SUPPLEMENTAL OPPOSITION TO
UNITED MICROELECTRONICS
CORPORATION'S MOTION TO DISMISS
FOR LACK OF PERSONAL JURISDICTION**

REDACTED VERSION OF DOCUMENT(S) SOUGHT TO BE SEALED

1 I, David Kuan-Yu Liu, declare as follows:

2 **I. INTRODUCTION AND QUALIFICATIONS**

3 1. My name is Dr. David Kuan-Yu Liu. I understand that I am submitting a
4 declaration in connection with Case No. 4:17-CV-06932-MMC before the United States District
5 Court, Northern District of California.

6 2. I have been retained by Jones Day as an expert to provide background on dynamic
7 random access memory (DRAM), to address technical issues and to offer technical opinions with
8 respect to Micron Technology, Inc.'s ("Micron") confidential information relating to its DRAM
9 devices and processes ("Micron's Confidential DRAM Technology") and certain patents and
10 patent applications filed by United Microelectronics Corporation ("UMC") and Fujian Jinhua
11 Integrated Circuit Co., Ltd. ("Jinhua") at the United States Patent and Trademark Office (the
12 "UMC/Jinhua Patent Filings").

13 3. As part of this work, I have been asked to review documents containing Micron's
14 Confidential DRAM Technology that I am informed UMC acquired without authorization along
15 with the UMC/Jinhua Patent Filings to determine what, if any, relationship exists between the
16 Micron's Confidential DRAM Technology and the UMC/Jinhua Patent Filings, including my
17 opinions on whether any of the UMC/Jinhua Patent Filings were based on or derived from
18 Micron's Confidential DRAM Technology. I have been asked to focus particularly on those
19 UMC/Jinhua Patent Filings where Chien-Ting Ho (also known as J.T. Ho) is a named inventor
20 and have been informed that J.T. Ho is a former Micron employee who was hired by and remains
21 employed at UMC and, while at UMC, was in possession of more than 20,000 computer files
22 containing Micron's Confidential DRAM Technology.

23 4. Based on my education, research, training and experience, as summarized further
24 below, I believe I am qualified to render expert opinions on the technical issues regarding
25 Micron's Confidential DRAM Technology and the UMC/Jinhua Patent Filings. My
26 compensation is not based on the outcome of my opinions.

27 5. It is my expert opinion that it is highly likely that the UMC/Jinhua Patent Filings
28 were based on and derived from the use of Micron's Confidential DRAM Technology. My

1 opinion is based on a comparison of the UMC/Jinhua Patent Filings and Micron's Confidential
2 DRAM Technology, and is buttressed by my consideration of the short period of time from when
3 UMC commenced working on DRAM technology and the priority dates of the UMC/Jinhua
4 Patent Filings, which make it highly unlikely that UMC/Jinhua independently developed the
5 structures, processing steps and techniques disclosed in the UMC/Jinhua Patent Filings.

6 6. My curriculum vitae (CV) is provided as **Exhibit 1** to this Declaration.

7 7. I am not a lawyer. As set forth in my CV, I hold M.S. and Ph.D. degrees in
8 Electrical Engineering from Stanford University and have 20 years of experience as an engineer
9 and engineering manager and director of Complementary Metal Oxide Semiconductor (CMOS)
10 technology development. I hold over 90 U.S. patents, a large number of which are directed to
11 CMOS processes and semiconductor process technology.

12 8. The vast majority of my patents are in the area of CMOS high-density circuit and
13 memory architecture. As such, I am intimately familiar with the concept of memory array
14 architecture and the key steps in the integrated process flow to manufacture high-density
15 memory devices, such as DRAM devices.

16 9. I have also authored several technical papers that have been published in
17 well-respected, peer-reviewed journals, such as the IEEE Electron Device Letters, the IEEE
18 Journal of Solid-State Circuits, and the IEEE Transactions on Electron Devices. As an example,
19 I worked on a new conductivity-modulated Power MOSFET that features a buried
20 minority-carrier injector to enhance the current conduction capability of the Power MOSFET.
21 This work was published in the IEEE Transactions on Electron Devices.

22 10. During my career, I have worked at some of the leading semiconductor
23 companies in the world, such as Texas Instruments, Advanced Micro Devices, Altera
24 Corporation (now a subsidiary of Intel Corp.), and Xilinx. At these companies, my work focused
25 on various aspects of CMOS and semiconductor process technology.

26 11. As result of my industrial experience, I have developed expertise in integrating
27 the different semiconductor process modules into a full process flow and bringing up the
28 integrated process flows into manufacturing and high yield production. I am fully cognizant of

1 the complexities and the many time-consuming experimental iterations required to fully resolve
2 all the process related yield-limiting issues that face modern semiconductor process designs.

3 12. I am not now and never have been an employee of Micron.

4 13. In writing this Declaration, I have considered the following: (1) my own
5 knowledge and experience, including my work experience in the fields of semiconductor design
6 and processes; (2) my experience in working with many others involved in those fields;
7 (3) Micron's Confidential DRAM Technology, which includes information that cannot be
8 reverse engineered such as Micron's DRAM processes and production parameters that must be
9 known and experimentally verified before chip production is possible, and which is detailed in
10 documents that I understand were in the possession of UMC before and when the UMC/Jinhua
11 Patent Filings were filed, including: (i) Micron DRAM 90 Series (25nm) Process Traveler
12 ("Micron 90 Series Traveler") (attached to the Declaration of Douglas L. Clark in Support of
13 Micron's Supplemental Opposition to UMC's Motion to Dismiss ("Clark Decl." Ex. 39); (ii)
14 Micron DRAM 100 Series (20nm) Process Traveler ("Micron 100 Series Traveler") (attached to
15 the Clark Decl. as Ex. 40); (iii) Elpida 25nm Process Flow Document ("Elpida Process
16 Document") (attached to the Clark Decl. as Ex. 41); and (iv) Micron Design Rules for DR25nm
17 ("Micron Design Rules") (attached to the Clark Decl. as Ex. 42); and (4) the UMC/Jinhua Patent
18 Filings, including specifically: (i) U.S. Patent No. 9,679,901 ("901 patent") (attached to the
19 Clark Decl. as Ex. 33); (ii) U.S. Patent Application No. 2018/0108563 ("563 Application")
20 (attached to the Clark Decl. as Ex. 34); (iii) U.S. Patent No. 9,973,790 ("790 patent") (attached
21 to the Clark Decl. as Ex. 35); (iv) U.S. Patent No. 9,929,162 ("162 patent") (attached to the
22 Clark Decl. as Ex. 36); and (v) U.S. Patent No. 9,859,283 ("283 patent") (attached to the Clark
23 Decl. as Ex. 38). As discussed above, I have specifically addressed these particular UMC/Jinhua
24 Patent Filings because Chien-Ting Ho (J.T. Ho) is a named inventor on these patent filings and
25 was in possession of more than 20,000 computer files containing Micron's Confidential DRAM
26 Technology while at UMC.

II. BACKGROUND OF DRAM PROCESS AND PRODUCT DEVELOPMENT

14. Due to the complexities in the manufacturing process flow for DRAM, it takes lengthy and iterative research and development, process technology development and product development cycles to successfully bring an advanced generation of DRAM chips into full production. This is especially true for a manufacturer entering into DRAM product development for the very first time, such as UMC/Jinhua, without the benefits of the experience gained from previous generations of DRAM manufacturing.

15. There is initial research, including for example benchmarking and competitive product analysis, for developing product specifications, where the desired specifications and performance parameters of the final DRAM product will be defined on a system and architectural level. Once this step is done, various functional elements that are required to implement and meet the specifications will be established in the form of requisite functional circuits. These proposed functional circuits dictate what elements on the device levels, or the transistor levels, are needed to build the requisite DRAM circuits. This aspect of the DRAM product development will drive and constrain the definition of electrical design rules for the various transistors and elements for the circuit design.

16. Just as importantly, the feature sizes—the physical or geometrical aspects—of the product will start to be defined by a set of dimensions referred to as geometrical “design rules.” These design rules are ultimately dictated by the process technology that is utilized. Integrated circuit devices are manufactured using a particular process technology node, which refers to the smallest dimension of a feature on the device, such as the dimension of a transistor gate. The smaller the process technology node, the more circuitry and functionality can be built into the device. Of course, the smaller the process technology node, the more advanced and complicated the process technology must be to successfully build a product that does not have defects. Because the capabilities and limitations of the process technology will determine what can and cannot be achieved, knowing the process technology is essential to defining these design rules.

17. Developing and deploying a new DRAM process technology is a massive undertaking that requires extensive research and development, determining the appropriate

1 process steps (hundreds of them) and the optimal sequence of and methods for implementing
2 those steps, selecting the semiconductor fabrication equipment to be used and integrating that
3 equipment into the process and more. Once the process technology node for the product is
4 determined, then a most aggressive (or competitive) and yet manufacturable unit cell area for the
5 DRAM memory array will be budgeted and conceptualized, in conjunction with formulating a
6 set of all the critical geometrical design rules that are needed to support and realize such a
7 DRAM unit cell. The geometrical design rules serve simultaneously as an enabler to
8 implement—within a given surface area of silicon—a competitive DRAM product featuring
9 memory cell arrays along with the supporting peripheral circuitry and design rules (both
10 electrical and geometrical) also provide directives for implementing the many processing steps
11 and the needed equipment to manufacture a DRAM product.

12 18. Given the critical importance of process technologies in manufacturing advanced
13 integrated circuits such as DRAM, the definition and successful delivery of the design rules is a
14 critical gateway in the development of a successful DRAM product. For example, if the design
15 rules are too aggressive and unrealistic for the selected process technology, the product will not
16 be manufacturable. But if the rules are too conservative, though the product may be highly
17 manufacturable by the selected process technology, it will not be competitive, for example, in
18 terms of the number of possible dies that can be placed on a given wafer due to its large size.
19 Companies like Micron, who have decades of experience on the process technologies and design
20 rules for multiple generations of DRAM devices, can leverage that foundation of experience to
21 develop new process technologies and design rules for the next generation DRAM products.
22 Even then, for a company that already has decades of experience in DRAM, developing and
23 deploying design rules and a new process technology node could easily take over two years.

24 19. After the design rules and fabrication process technologies are in place, the circuit
25 design is then implemented according to the geometrical design rules into a set of mask patterns
26 that will be used to build onto the silicon wafer the DRAM chips, which include memory cell
27 arrays and the periphery circuits. The process of implementing the circuit designs into
28 geometrical features on the mask patterns is known as the layout of the circuit design.

20. The hundreds of fabrication process steps, which involve a variety of highly-complex semiconductor processing techniques such as diffusion, etching, ion implantation, and photolithography patterning etc., are then coupled together as a sequence of well-engineered and intended process steps, known as the “process flow,” and optimized “recipes” are used to implement the various process steps making up the process flow. The silicon wafers can be thought of as the vehicle that will “travel” through the process flow, with each process step contributing to building of the DRAM chips onto a silicon wafer. These process steps, including their sequence along the process flow, are detailed and documented in what are sometimes known as “traveler” files, and in what Micron calls a “process traveler,” that literally capture years (if not decades) of research, development and iterative experimentation. The primary high-level modules of the DRAM process flow are: (i) building the isolation structures that demarcate the moat area from the active device elements areas; (ii) forming the access transistors, or the Word Line transistors, buried under the surface of the silicon wafer to address the memory cells; (iii) building the Bit Line connection and Bit Lines to address the memory cells; (iv) forming reliable connecting structures in a very tight space to contact to the storage nodes of the DRAM memory cells; and (v) forming capacitors that are in the shape of tall cylindrical containers. It should be mentioned that many of the process steps, and the sequence of those process steps required to build advanced DRAM circuits are very different from and much more complex than the steps to build logic circuits.

21. Once the silicon wafers have gone through all the steps in the process flow, the completed DRAM chips are tested while they are still in the form of dies on the wafers. The wafers are then cut into many individual dies with the test-proven functional dies being packaged into chips. The packaged parts are then tested again to ensure the dies survived the packaging process. These final packaged parts are the individual DRAM chip that are typically incorporated into a memory module.

22. Based on my experience in the semiconductor industry as a process integration engineer, and my experience bringing many generations of semiconductor processes for manufacturing memory integrated circuits to full production, I am intimately familiar with the

1 necessary research, development, experimentation and trial-and-error approach required to
2 support the implementation of new process improvement and manufacturing methods. These
3 new process methods, whether they are new layout methods, new process steps, or new process
4 chemistry and sequence, are all meant either to address certain issues that otherwise would limit
5 the manufacturability of the integrated circuits, or to simplify the process steps and reduce the
6 cost of manufacturing.

7 23. For a company that is developing complex integrated circuits, such as DRAM
8 memory integrated circuits, there typically exists an established baseline process or experimental
9 metrics that would lead an engineer to understand and potentially develop process
10 improvements. This is especially true in the highly complex and expensive integrated circuit
11 manufacturing processes. The requirements for improvement first need to be realized and
12 understood, the quantifiable benefits from the improved methods also need to be demonstrated
13 before the manufacturing process flow can adopt the new, improved method and for the
14 company to even begin to understand the capabilities and limitations of the new methods.

15 24. Based on my experience in this area working with many integrated circuit
16 manufacturing companies, it would be extremely unlikely for any company to come up with new
17 process improvements and manufacturing methods without the prerequisite learning and data
18 from many iterations of experiments on the actual process flow. In addition, these improvements
19 are typically learned through many experiments performed on prototype chips that have been
20 fabricated to resemble the final products as closely as possible so that any meaningful
21 observations and improvements are directly applicable to the final products.

22 25. Using the background described above as a perspective, I have examined the
23 UMC/Jinhua Patent Filings to assess the likelihood that the descriptions, disclosures and claimed
24 inventions were based on UMC/Jinhua's independent development of the DRAM process
25 technologies described therein in view of the following timeline in relation to the priority dates
26 of the UMC/Jinhua Patent Filings:

- 27 • December 2015 – UMC lacked experience in DRAM technology, and other than
28 several former Micron employees who recently joined UMC, UMC had few, if any,

engineers experienced in DRAM technology.

- January 2016 – UMC and Jinhua enter a joint agreement to develop DRAM technology.
- July or August 2016 – Kenny Wang at UMC is tasked with developing UMC’s design rules for F32 25nm DRAM technology.¹
- September 2016 – Design rules by UMC were completed.²
- September 22, 2016 – Priority date of the ‘901 Patent.
- October 17, 2016 – Priority date of the ‘563 Application.
- December 9, 2016 – Priority date of the ‘790 Patent.
- December 22, 2016 – Priority date of the ‘162 Patent.
- March 7, 2017 – Priority date of the ‘283 Patent.

III. ANALYSIS OF UMC/JINHUA PATENT FILINGS AND SIMILARITIES TO MICRON’S CONFIDENTIAL DRAM TECHNOLOGY

A. UMC/Jinhua United States Patent 9,679,901

26. The ‘901 Patent is titled “Semiconductor Device and Manufacturing Method Thereof.” It was filed in the United States Patent Office on October 18, 2016, and claims priority to a Chinese application filed on September 22, 2016. The patent includes 3 drawings and 10 claims. Chien-Ting Ho (J.T. Ho) is one of the named inventors listed on the front page of the ‘901 Patent.

27. The ‘901 Patent describes a semiconductor device, that includes a substrate, a plurality of active areas, and an isolation structure, as well as a manufacturing method of a semiconductor device, and specifically references “the existing DRAM process.” (‘901 Patent at Abstract; 2:10-43; 5:49-50) The “Description of Embodiments” section of the ‘901 Patent is

¹ According to the Indictment Decision of Taiwan Taichung District Prosecutors Office, attached as Exhibit 2 to Micron’s Complaint, September 2016 is the earliest UMC completed its design rules. The Indictment Decision states that “in July or August 2016” Kenny Wang, another former Micron employee who joined UMC, was asked to work on UMC’s design rules, that Wang used the Micron design rules he took to UMC to work on the UMC design rules and that the “design rules were completed within only 2 months and handed to the chip design manufacturer for the next step.” Micron Complaint, Ex. 2, pp. 6-7.

² *Supra* note 1.

1 specifically directed towards DRAM process technology, including specific steps directed
2 towards layout, patterning, active area formation, etching, oxide deposition, trench formation,
3 and other process and design steps. ('901 Patent at 3:10 – 5:67)

4 28. In the background section, the '901 Patent explains that “in the current
5 semiconductor process, an isolation structure is generally formed in a substrate to define a device
6 region having a plurality of active areas and a peripheral region. Due to miniaturization of the
7 semiconductor device, the device region becomes smaller, and “a greater difference in pattern
8 density results on the substrate, and the difference in pattern density becomes an issue in a
9 subsequent process.” ('901 Patent at 1:25-30). This negative effect from the difference in
10 pattern density is more significant at the interface region of the device region and the peripheral
11 region, due to various stresses caused by the difference in pattern density.

12 29. The '901 Patent purports to provide an improved process that is capable of
13 preventing the effect of this stress being generated by introducing features at the edges of the
14 ends of the active area adjacent to the boundary of the device region. Figure 2A of the
15 '901 Patent illustrates an embodiment of the claimed inventions, and shows “the ends of the last
16 active areas 106 in each row have a greater width in comparison to the other portions.” ('901
17 Patent at 5:8-10) The manufacturing method described in the '901 Patent discloses the capability
18 of preventing the negative effect on subsequent processing steps caused by the difference in
19 pattern density in the active areas. That capability would need to be substantiated by actual
20 experimental results on a working process flow to determine tangible and observable results of
21 whether an effect on a subsequent process is prevented. It is also reasonable to conclude that the
22 layout of the memory array active area would have already been determined and implemented in
23 order to provide the disclosures set forth in the '901 Patent.

24 30. The claims of the '901 Patent include both product and method claims. Claims 1-
25 5 are directed to a semiconductor device that includes a substrate having a device region and a
26 peripheral region, a plurality of device active areas, and an isolation structure, where the design
27 of the active areas is such that the edges of the ends of the active areas adjacent to the device
28 region are aligned with each other and a width of the ends of the active areas adjacent a boundary

1 of the device region is greater than a width of other portions of the active areas. Claims 6-10
2 recite methods for manufacturing such a semiconductor device.

3 31. The '901 Patent describes the same or very similar process technology as
4 described in Micron's Confidential DRAM Technology that I understand was in UMC's
5 possession. Like the later-filed '901 Patent, [REDACTED]

6 [REDACTED]

7 [REDACTED]

8 [REDACTED]

9 [REDACTED]

10 [REDACTED]

11 [REDACTED]

12 [REDACTED] again similar to what was later described in the '901 Patent.

13 32. In my opinion, it is highly likely that the disclosures and purported inventions set
14 forth in the '901 Patent were derived from or based on Micron's Confidential DRAM
15 Technology. In addition, in order for the UMC/Jinhua inventors to get to a stage in development
16 where they could disclose the detailed DRAM process steps and structures set forth in the
17 '901 Patent, not only would they have needed completed design rules for their DRAM product,
18 but they would also need to have completed multiple complex processing steps in the process
19 flow, and would then need to run process experiments up to the point where the structures shown
20 in the '901 Patent were built. In view of the fact that UMC did not even have design rules
21 completed until September, 2016 and that the priority date of the '901 Patent is September 22,
22 2016, it is highly unlikely that UMC/Jinhua independently developed the subject matter
23 described in the '901 Patent.

24 **B. UMC/Jinhua United States Patent Application 2018/0108563**

25 33. The '563 Application is titled "Method of Fabricating Isolation Structure." It was
26 filed in the United States Patent Office on December 20, 2016, and claims priority to a Chinese
27 application filed on October 17, 2016. It includes 27 drawings and 10 claims. Chien-Ting Ho
28 (J.T. Ho) is one of the named inventors listed on the front page of the '563 Application. Fu-Che

1 Lee is also a named inventor on the '563 Application and I understand Mr. Lee is also known as
2 Neil Lee and is a former Micron employee who subsequently was hired by UMC.

3 34. The '563 Application describes a specific method of fabricating a semiconductor
4 device, and particularly relates to a method of fabricating an isolation structure using a specific
5 "double patterning" technique. The application discloses a technique to form spaces that are
6 smaller than the dimension of the features on the mask using a series of patterned hard mask
7 layers and oxide layers to ultimately form trench patterns in the semiconductor substrate. ('563
8 Application at Abstract) This type of technique is also known as "pitch doubling."

9 35. In the background section, the '563 Application states that "to achieve high
10 density and high performance goals with an increased degree of integration of a semiconductor
11 device, it is preferable to manufacture a structure having a smaller size and higher degree of
12 integration." ('563 Application at 1:0003) To manufacture such a structure, the
13 '563 Application describes forming an isolation structure in the substrate where trenches are
14 formed in the substrate first, and then an isolation material is filled in the trenches. When
15 manufacturing DRAM integrated circuits, however, different widths of the trenches will lead to a
16 big difference in the width of the shallow trench isolation (STI) between the memory array
17 region and the periphery region, resulting in non-uniform pattern density and large height
18 differences on the surface of the substrate, and this non-flat profile affects subsequent process
19 steps. ('563 Application, at 1-2)

20 36. The '563 Application purports to provide an improved process to address this
21 problem and describes process steps that essentially use the sidewall of a feature on the mask to
22 define a very small opening as the trench opening within the memory active region, and use
23 another mask to open up wider spaces in the periphery region, such that different STI widths can
24 be obtained in manner resulting in a substrate with a flat profile for subsequent process steps.
25 (Ex. 8 at 1-3) These "pitch doubling" process steps are also illustrated in the '563 Application:
26 figure 1C shows that a spacer layer is formed with patterned hard mask layers and planarized;
27 figure 1D illustrates that an etch process is performed that only removes the spacer layer and
28 forms an opening of the narrow trenches in the memory array region, and; figure 1F illustrates

1 that an additional hard mask layer is used to form wider openings for wider trench openings.
2 ('563 Application, Figures 1C, 1D and 1F)

3 37. Claim 1 of the '563 Application recites a method of fabricating an isolation
4 structure by forming a first oxide layer and a second oxide layer and also forming first, second
5 and third hard mask layers. By removing and patterning these layers the claim recites forming
6 trench patterns with different widths. The sequence of steps and the layers set forth in claim 1 of
7 the '563 Application result in a doubling of the pitch achievable over standard patterning for
8 trench formation by using a sidewall spacer region as the opening for the trench. ('563
9 Application at Claim 1)

10 38. The '563 Application describes the same or very similar process technology as
11 described in Micron's Confidential DRAM Technology that I understand was in UMC's
12 possession. The method described in the later-filed '563 Application [REDACTED]

13 [REDACTED]
14 [REDACTED]
15 [REDACTED]
16 [REDACTED]
17 [REDACTED]
18 [REDACTED]
19 [REDACTED]
20 [REDACTED]
21 [REDACTED]
22 [REDACTED]
23 [REDACTED]
24 [REDACTED]
25 39. Additional overlap between the later-filed '563 Application and Micron's
26 Confidential DRAM Technology [REDACTED]

27 [REDACTED] The '563 Application shows that the narrow
28 trenches are filled with a first layer of dielectric material, while the wide trench is filled with two

different separate steps of depositing the dielectric material. ('563 Application, at Fig. 5E) [REDACTED]

[REDACTED]
[REDACTED]
[REDACTED] The same similarities described above
are also found when comparing the later-filed '563 Application to [REDACTED]
[REDACTED]

40. In my opinion, it is highly likely that the disclosures and inventions set forth in the '563 Application were derived from or based on Micron's Confidential DRAM Technology. In addition, in order for the UMC/Jinhua inventors to get to a stage in development where they could disclose the detailed double-patterning trench formation process and the subsequent specific trench filling process steps described in the '563 Application, they would have needed completed design rules for their DRAM product, masks to implement the different trench widths in the array and the periphery, a completed STI formation module, and they would have then needed to perform SEM cross sections to visually ensure that the trench formation steps were operational. In view of the fact that UMC did not have design rules completed until September, 2016 and the priority date of the '563 Application is October 17, 2016, it is highly unlikely that UMC/Jinhua independently developed the subject matter described in the '563 Application.

C. UMC/Jinhua United States Patent 9,973,790

41. The '790 Patent is titled "Semiconductor Device and Method for Forming the Same." It was filed in the United States Patent Office on March 13, 2017, and claims priority to a Chinese application filed on December 9, 2016. The patent includes 6 drawings and 12 claims. Chien-Ting Ho (J.T. Ho) is the first listed inventor on the front page of the '790 Patent.³

42. The '790 Patent describes a semiconductor device that includes a substrate including a memory region and a plurality of memory cells formed in the memory region, a plurality of first and second connecting structures, and a plurality of dummy nodes and storage

³ J.T. Ho is also a named inventor on U.S. Patent No. 9,960,167, which is a divisional of the '790 Patent. The '167 and '790 Patents have the same priority date (December 9, 2017) and have essentially the same patent specification. For purposes of brevity, I have limited my discussion to the '790 Patent, but my discussion and opinions in connection with the '790 Patent apply equally to the '167 Patent.

1 nodes. The dummy nodes are disposed on the first connection structures and the storage nodes
2 are disposed on the second connection structures. ('790 Patent, at Abstract)

3 43. The background section of the '790 Patent identifies the problem that "as memory
4 cells of DRAM become more integrated and miniaturized, fabrication of these elements becomes
5 more difficult." DRAM integrated circuits include arrays of memory cells with high pattern
6 density, and also include logic devices in the peripheral regions, with a very different pattern
7 density. The different device densities "between the memory cells and the logic devices further
8 induce process issue." ('790 Patent at 1:5-50)

9 44. The '790 Patent purports to address this problem by disclosing a semiconductor
10 device that includes "a plurality of dummy nodes" respectively disposed on first connecting
11 structures, whereas a plurality of first storage nodes of the regular memory cells are respectively
12 disposed on second connecting structures. ('790 Patent at Abstract and Claim 1) The connecting
13 structures disclosed in the '790 Patent include a conductive portion and a metal portion, with the
14 conductive portion being sandwiched between the metal portion and the substrate. According to
15 the '790 Patent, the first connecting structures being electrically connected to the dummy nodes
16 are formed on the substrate of the memory region to increase the pattern density, and solve the
17 process issue induced by different pattern densities. ('790 Patent at 1:55-2:47) Figure 5 of the
18 '790 Patent illustrates both the first connecting structure and the second connecting structure
19 respectively connecting the dummy nodes or the storage node to the substrate. ('790 Patent at
20 Fig. 5) The '790 Patent also describes specific DRAM memory cell manufacturing steps as
21 follows: A plurality of shallow trench isolation ("STI") structures are formed in the substrate in
22 the memory region and the peripheral region. Next, a plurality of recesses are formed in the
23 substrate and the STI structures in the memory region. A dielectric layer is then formed to cover
24 sidewalls and bottoms of the recesses. Thereafter a buried gate is formed in each recess and
25 followed by forming an insulating layer to seal each recess. Next, a source/drain region is
26 formed in the substrate at two sides of the buried gates. ('790 Patent at 3:55-4:3)

27 45. Claim 1 of the '790 Patent recites a semiconductor device comprising a substrate
28 having a memory region and a plurality of memory cells, a plurality of first and second

1 connecting structures, a plurality of first storage nodes and a plurality of dummy nodes. The first
2 storage nodes are disposed on the second connecting structures and the dummy nodes are
3 disposed on the first connecting structures. The first and second connecting structures have
4 conducting portions and metal portions but the height of the metal portions is different between
5 the two connecting structures.

6 46. The '790 Patent describes the same or very similar process technology as
7 described in Micron's Confidential DRAM Technology that I understand was in UMC's
8 possession. Like the later-filed '790 Patent, [REDACTED]

9 [REDACTED]
10 [REDACTED]
11 [REDACTED]
12 [REDACTED]
13 [REDACTED]
14 [REDACTED]
15 [REDACTED]
16 [REDACTED]
17 [REDACTED]
18 [REDACTED]
19 [REDACTED]
20 [REDACTED]
21 [REDACTED], again

22 similar to what was later described in the '790 Patent.

23 47. In my opinion, it is highly likely that the disclosures and inventions set forth in
24 the '790 Patent were derived from or based on Micron's Confidential DRAM Technology. In
25 addition, in order to implement the normal storage node connecting structure and the dummy
26 connecting structure in a manner that addresses the pattern density issue as described in the
27 '790 Patent, the array pattern density in the UMC/Jinhua DRAM technology would need to be
28 final, or close to final, in order to facilitate the observation of any meaningful process issue that

would mirror the real product. Also given that there is a difference in the step height of metal portions of the connecting structures, it would be reasonable to conclude that the stated benefits of the invention described in the ‘790 Patent would need to be observable on actual DRAM cells that feature the connecting structures that connect between the DRAM capacitors and the storage nodes of the memory access transistor. Thus, in order for the UMC/Jinhua inventors to get to a stage in development where they could disclose the detailed DRAM process steps, array formation and connecting structures set forth in the ‘790 Patent, not only would they have needed completed design rules for their DRAM product, but they would also need mask patterns, mostly completed process modules, and to have actually run the connecting structure formation module to implement the different step heights in the metal portion and in order to quantify any benefits. In view of the fact that UMC did not have design rules completed until September, 2016 and the priority date of the ‘790 Patent is December 9, 2016, it is highly unlikely that UMC/Jinhua independently developed the subject matter described in the ‘790 Patent.

D. UMC/Jinhua United States Patent 9,929,162

48. The ‘162 Patent is titled “Semiconductor Device and Method for Forming the Same.” It was filed in the United States Patent Office on March 12, 2017, and claims priority to a Chinese application filed on December 22, 2016. It includes 17 drawings and 18 claims. Chien-Ting Ho (J.T. Ho) is one of the named inventors listed on the front page of the ‘162 Patent.

49. The ‘162 Patent describes a semiconductor device that includes a memory cell region, an isolation mesh, and a plurality of storage node contact plugs that are formed within apertures of the isolation mesh structure as well as a manufacturing method of forming a semiconductor device. (‘162 Patent at Abstract; 1:59 – 2:50)

50. The ‘162 Patent makes clear that it is particularly related to DRAM and identifies the problem that “as memory cells of DRAM become more integrated and miniaturized, overlay margin between the contact plugs for providing electrical connection to the storage node and to the bit line is reduced,” causing a process issue and resulting in process yield deficiency. (‘162 Patent at 1:15-55; 2:46-50). The ‘162 Patent purportedly addresses this problem by disclosing a

1 semiconductor device that includes “at least a memory cell region defined therein, and isolation
2 mesh formed on the substrate and a plurality of storage node contact plugs.” The isolation mesh
3 “includes a plurality of essentially homogeneous dielectric sidewalls and a plurality of first
4 apertures defined by the sidewalls. The storage node contact plugs are formed in the first
5 apertures...” (‘162 Patent at 1:59-2:3). According to the ‘162 Patent, because the isolation mesh
6 includes the apertures and the storage node contact plugs are subsequently formed in the
7 apertures, the storage node contact plugs are physically spaced apart and electrically isolated
8 from the bit line contact plugs and the bit lines by a reliably controlled spacing, which provides
9 an improvement in the process yield. (‘162 Patent at 2:36 -2:50) Figure 7 of the ‘162 Patent
10 illustrates how the isolation mesh isolates the bit line connections. The ‘162 Patent also
11 discloses a specific set of process steps whereby after forming the isolation mesh, the etch stop
12 layer exposed at the bottoms of the apertures is removed to expose the source region of the
13 memory cells . Subsequently, a storage node contact plug is formed, and the bit lines are
14 physically spaced apart and electrically isolated form the storage nodes by the dielectric
15 sidewalls. (‘162 Patent at 6:5-15)

16 51. Claim 1 of the ‘162 Patent recites a semiconductor device comprising a substrate
17 having a memory cell region and a plurality of memory cells, an isolation mesh having columns
18 and ribs formed of dielectric, and a plurality of storage node contact plugs formed in apertures of
19 the isolation mesh.

20 52. The ‘162 Patent describes the same or very similar process technology as
21 described in Micron’s Confidential DRAM Technology that I understand was in UMC’s
22 possession, including the [REDACTED]

23 [REDACTED] Like the later-filed ‘162 Patent, [REDACTED]
24 [REDACTED]
25 [REDACTED]
26 [REDACTED]
27 [REDACTED]
28 [REDACTED]

1 [REDACTED]
2 [REDACTED]
3 [REDACTED]
4 [REDACTED]
5 [REDACTED], again similar to what was later described in the '162 Patent.

6 53. In my opinion, it is highly likely that the disclosures and inventions set forth in
7 the '162 Patent were derived from or based on Micron's Confidential DRAM Technology. In
8 addition, the problem the '162 Patent purports to address is an issue that occurs at the back
9 portion of the DRAM memory cell formation as the assurance of electrical connection being
10 provided to the storage node can only be ascertained by measurement between the source node
11 and the storage capacitor. Thus, in order for the UMC/Jinhua inventors to get to a stage in
12 development where they could disclose the detailed DRAM process steps and structures set forth
13 in the '162 Patent, a fully functional DRAM cell array would likely be required to observe the
14 yield enhancement benefits described in the '162 Patent. Not only would the UMC/Jinhua
15 inventors have needed completed design rules for their DRAM product, but they would also need
16 to have masks generated that would allow the engineers to optimize the size of the isolation mesh
17 and apertures, both of which would require the layout of the memory cell arrays to be known in
18 order to determine the tight layout dimensions for forming these mesh and apertures as disclosed
19 in the '162 Patent. In view of the fact that UMC did not have design rules completed until
20 September, 2016 and the priority date of the '162 Patent is December 22, 2016, it is highly
21 unlikely that UMC/Jinhua independently developed the subject matter described in the
22 '162 Patent.

23 **E. UMC/Jinhua United States Patent 9,859,283**

24 54. The '283 Patent is titled "Semiconductor Memory Structure." It was filed in the
25 United States Patent Office on April 5, 2017, and claims priority to a Chinese application filed
26 on March 7, 2017. It includes 12 drawings and 18 claims. Chien-Ting Ho (J.T. Ho) is one of the
27 named inventors listed on the front page of the '283 Patent.

28 55. The '283 Patent describes a semiconductor memory structure, and more

1 particularly a DRAM semiconductor structure, that includes a memory cell region, a peripheral
2 region, and a cell edge region. The structure also includes a plurality of active regions formed in
3 these regions and at least a dummy bit line formed on the active regions of the cell edge region.
4 ('283 Patent at Abstract; 1:7-10)

5 56. In the background section, the '283 Patent identifies the problem that "DRAM
6 includes not only the memory cells that are arranged in array-like manner in the memory region
7 but also other logic devices that are formed in the non-memory/peripheral region," and that "the
8 different device densities between the memory cells and the logic devices further induce process
9 issue." ('283 Patent at 1:47-52)

10 57. The '283 Patent purports to address the problems arising from different device
11 densities between the memory cells and the logic devices by including "at least a dummy bit line
12 formed on the active regions in the cell edge region," and this dummy bit line is extended along a
13 "first direction and overlaps at least two active regions along a second direction." ('283 Patent at
14 Abstract and claim 1) The dummy bit line in the cell edge region is described and illustrated in
15 the '283 Patent and also includes contact plugs which include a polysilicon layer and a metal-
16 containing layer. ('283 Patent at Figs. 7A, 7B, and 4:1-10) The '283 Patent also shows buried
17 word lines running in the vertical direction and a bit line contact placed between two adjacent
18 word lines that are crossing the same cell active area. ('283 Patent at Fig. 1A which shows cell
19 active areas as the pill shape features going diagonally across)

20 58. Claim 1 of the '283 Patent recites a substrate, a plurality of active regions, and a
21 dummy bit line formed on the active regions. More specifically claim 1 recites that the dummy
22 bit line is extended in a first direction and overlaps active regions oriented in a second direction
23 perpendicular to the first direction. The claim also recites further aspects of the dummy bit lines
24 including a width of the first inner line portion being different from the second inner line portion.
25 ('283 Patent at 7:40-58)

26 59. The '283 Patent describes the same or very similar process technology as
27 described in Micron's Confidential DRAM Technology that I understand was in UMC's
28 possession. Like the later-filed '283 Patent, [REDACTED]

1 [REDACTED]
2 [REDACTED]
3 [REDACTED]
4 [REDACTED]
5 [REDACTED]
6 [REDACTED]
7 [REDACTED]
8 [REDACTED]
9 [REDACTED]
10 [REDACTED] just as described and claimed as the purported invention in the
11 '283 Patent.

12 60. In my opinion, it is highly likely that the disclosures and purported inventions set
13 forth in the '283 Patent were derived from or based on Micron's Confidential DRAM
14 Technology. In addition, in order for the UMC/Jinhua inventors to get to a stage in development
15 where they could disclose the detailed DRAM process steps and in particular the dummy bit line
16 structures in the '283 Patent, not only would they have needed completed design rules for their
17 DRAM product, but they would also need to have been close to a final pattern density and close
18 to final process steps for producing these structures to make any meaningful decision regarding
19 these techniques. In view of the fact that UMC did not have design rules completed until
20 September, 2016 and the priority date of the '283 Patent is March 7, 2017, it is highly unlikely
21 that UMC/Jinhua independently developed the subject matter described in the '283 Patent.

22 **IV. CONCLUSIONS**

23 61. Given the substantial similarity and significant overlap between the UMC/Jinhua
24 Patent Filings and Micron's Confidential DRAM Technology, the complexity of the technology
25 involved and that UMC was in possession of significant amounts of Micron's Confidential
26 DRAM Technology from the beginning of UMC's DRAM development continuing through the
27 priority filing dates of the UMC/Jinhua Patent Filings, in my opinion it is highly likely that
28 UMC/Jinhua Patent Filings were derived from and based on Micron's Confidential DRAM

1 Technology. Furthermore, based on my 20+ years of memory process integration experience in
2 the semiconductor industry, it is highly unlikely that the purported inventive features and
3 techniques disclosed by the inventors in the UMC/Jinhua Patent Filings are based on
4 independent development that could have been learned and acquired during the short time period
5 between the beginning of UMC's DRAM development and the priority filing dates of the
6 UMC/Jinhua Patent Filings.

7
8 I declare under penalty of perjury under the laws of the United States of America that the
9 foregoing is true and correct to the best of my knowledge and belief.

10
11 Executed on this 12th day of August 2018, in Fremont, California.

12
13 By: 

14 David Kuan-Yu Liu, Ph.D.

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17 NAI-1504136938
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EXHIBIT 1

DAVID KUAN-YU LIU, Ph.D.

42063 Benbow Drive, Fremont, CA 94539 • (510) 770-9449 or (510) 579-5029
www.davidkyliu.com davidkyliu@comcast.net

PROFESSIONAL PROFILE

- Technical expert with over 20 years of experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Consultant and expert witness for semiconductor intellectual property evaluation and patent litigation, with successful deposition experience.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

EXPERT WORK EXPERIENCE:

Case: *Macronix vs. Toshiba*

Jurisdiction: Investigation No. 337-TA-1046
United States International Trade Commission

Work Product: Testifying expert for 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, deposition taken for 2 patents, issued witness statement and rebuttal witness statement, testified in ITC court on both infringement and invalidity.

Nature of Case: ITC infringement case concerning advanced NAND Flash memory array architecture.

Counsel: Retained by Fish Richardson (Contact: David Barken)

Date: 4/17 – Current

Case: *Novatek Microelectronics Corp. IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)
Date: 2/17 – 4/17

Case: *Taiwan Semiconductor Manufacturing Company IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: John Goetz)
Date: 7/15 – 4/17

Case: *Triune Systems, LLC vs. Wayne Chen, et al.,*
Jurisdiction: Cause No. 296-03209-2013, 296 District Court of Collin County, TX
United States International Trade Commission
Work Product: Testifying expert, database viewing, expert report, video-taped testimony
Nature of Case: Defending against trade secret contention.
Counsel: Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date: 5/15 – 9/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-922
United States International Trade Commission
Work Product: Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 9/14 – 1/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-909
United States International Trade Commission
Work Product: Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Winston & Strawn (Contact Michael Murray)
Date: 5/14 – 1/15

Case: *Keranos, LLC v. Analog Devices et. al.*
Jurisdiction: Civil Case No. 2:10-CV-00207
United States District Court for the Eastern District of Texas
Work Product: Claim Chart Generation and Claim Construction
Nature of Case: Patent infringement case concerning split gate Flash memory cell
Counsel: Retained by Agility IP (Contact Michelle Breit)
Date: 2/09 – 2/14

Case: **Silicon Storage Technology, Inc. v. Xicor, LLC**
Jurisdiction: Civil Case No. CV 10-01515
United States District Court for the Northern District of California
Work Product: Expert report, and declarations
Nature of Case: Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: **Fast Memory Erase, LLC v. Spansion et.al.**
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: **Fast Memory Erase, LLC v. Spansion et.al.**
Jurisdiction: Civil Case No. 3-08cv0977M
United States District Court for the Northern District of Texas
Work Product: Expert report, declarations, and depositions
Nature of Case: Patent infringement case concerning minimizing source current during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

EXPERIENCE:

10/07 to present: **Technical Consultant**

Fish & Richardson, Serving as a testifying expert for the case of Macronix vs. Toshiba. Case involvement ended in ITC trial testifying for infringement and invalidity. Responsible for reviewing layout database in GDS formation and studying circuit schematics for gathering and reviewing of evidence, both for DI purpose and for infringement purpose.

Gordon & Rees LLP, Served as a testifying expert for trade secret contention case of Triune Systems vs. Wayne Chen, *et al.*, Case ended in settlement after summary jury trial. Responsible for gathering and reviewing of evidence, analyzed integrated circuits for technology features, issuing expert report, and video taped jury trial testimony.

Fish & Richardson, Served as a testifying expert for the case of Macronix vs. Spansion. Case ended in settlement. Responsible for gathering and reviewing of evidence, both for DI purpose and for infringement purpose, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report.

Winston & Strawn. Served as a consulting expert for the case of Macronix vs. Spansion. Case ended in settlement. Responsible for gathering and reviewing of evidence, both for DI purpose and for infringement purpose.

ShoreChanBragalone. Served as an expert witness for the case of Intersil vs. SST. Summary judgment was granted after claim charts and infringement contention were generated.

Keranos. Serving as an expert witness for the case of Keranos, LLC vs. Analog Devices, Inc. et. al. Overseeing the generation of claim charts and coordinating efforts in reverse engineering work on integrated circuit products.

ShoreChanBragalone. Served as an expert witness and testifying witness for the case of Fast Memory Erase, LLC vs. Spansion *et al.* (Performed claim construction, provided deposition testimony, and wrote expert report.)

RPX Corporation. Evaluated flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent (total 76 patents) and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets.

IBM Corp. Reviewed and evaluated IBM's 180nm HV process technology against customer's IP and applications, with a view toward IBM's potential bid for customer's process technology offerings. Assessed process compatibility and outlined gap/overlaps between IBM and customer.

Law+. Worked as a technical expert for the lead attorney on several IP litigation cases in the area of flash memory and CMOS process technology. Assembled critical evidence to invalidate key patent claims. Generated claim charts for several patents.

10/07 to 4/11:

Jonker, LLC

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07:

Maxim Integrated Products, San Jose, California

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35µm and 0.18µm CMOS technology nodes. Analyzed and solved process-related reliability issues.

- 5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**
Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.
- 2/00 to 5/00 **Progressant Technologies, Fremont, California**
Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.
- 9/98 to 2/00 **Programmable Silicon Solutions, Sunnyvale, California**
Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.
- 9/97 to 9/98 **AMIC Technology, Santa Clara, California**
Director of Flash Technology. Responsible for developing 0.35 μ m ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.
- 5/96 to 9/97 **Altera Corp., San Jose, California**
Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35 μ m generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.
- 7/95 to 5/96 **Information Storage Devices, San Jose, California**
Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.
- 5/92 to 7/95 **Advanced Micro Devices, Sunnyvale, California**

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5 μ m and 0.35 μ m flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92

Texas Instruments, Dallas, Texas

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983

AEA Faculty Development Fellowship, 1983-1985

AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K.-L. Chen and H. Tigelaar), issued April 21, 1992.
2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.
3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.
4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.
5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.
6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.
7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.
8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.
9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994
10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.
11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.
12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.
13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.
14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.
15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.
16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.
17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.

18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.
19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.
20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.
21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.
22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.
23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.
24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.
25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997
26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.
27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.
28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.
29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998
30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.
31. U.S. Patent 5,814,854, "Highly scalable FLASH EEPROM cell," Issued September 29, 1998.
32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.
33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.
34. U.S. Patent 5,930,174, "Circuit and Method for Erasing Flash Memory Array," Issued July 27, 1999.
35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.

36. U.S. Patent 5,995,418, "Circuit and Method for Erasing Flash Memory Array," Issued November 30, 1999.
37. U.S. Patent 6,026,017, "Compact nonvolatile memory," Issued February 15, 2000.
38. U.S. Patent 6,027,974, "Nonvolatile memory," Issued February 22, 2000.
39. U.S. Patent 6,088,263, "Non-volatile memory using substrate electrons," Issued July 11, 2000.
40. U.S. Patent 6,091,636, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued July 18, 2000.
41. U.S. Patent 6,127,225, "Memory cell having implanted region formed between select and sense transistors," Issued October 3, 2000.
42. U.S. Patent 6,159,800, "Method of forming memory cell," Issued December 12, 2000.
43. U.S. Patent 6,188,604, "Flash memory cell & array with improved pre-program and erase characteristics," Issued February 13, 2001.
44. U.S. Patent 6,185,133, "Flash EPROM using junction hot hole injection for erase," Issued February 6, 2001.
45. U.S. Patent 6,252,799, "Device with embedded Flash and EERPOM memories," Issued June 26, 2001.
46. U.S. Patent 6,326,265, "Device with Embedded Flash and EPROM Memories," Issued December 4, 2001.
47. U.S. Patent 6,417,550, "High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage," Issued July 9, 2002.
48. U.S. Patent 6,479,862, "Charge trapping device and method for implementing a transistor having a negative differential resistance mode," Issued November 12, 2002.
49. U.S. Patent 6,512,274, "CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same," Issued January 28, 2003.
50. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device," Issued July 22, 2003.
51. U.S. Patent 6,624,026, "Nonvolatile Memory," Issued September 23, 2003.
52. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process," Issued January 20, 2004.
53. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same," Issued February 3, 2004.
54. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR) characteristic," Issued February 17, 2004.
55. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold," Issued March 2, 2004.

56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.
57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.
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